A3 cancel D' cont'd

storing the parasitic information in an accessible format; and

creating the wire load model dependent on the parasitic information.

sub D' 7

19. (Amended) A wire load model creation tool, comprising:

means for creating an interconnection configuration for a structure;

A4

means for field solving the interconnect configuration to determine parasitic information, wherein the parasitic information comprises capacitance and resistance information;

means for storing the parasitic information;

curve-fitting means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model; and

means for controlling error in the curve-fitting means.

Please add new claim 20.

A5 D' 7

20. The method of claim 1, wherein the interconnect configuration is non-symmetrical.--

REMARKS

Please reconsider the application in view of the above amendments and the following remarks.

I. Disposition of Claims

Claims 1-19 are pending in the instant application. Claims 1, 6, 11-15, and 19 have been amended and new claim 20 has been added.

II. Claim Amendments

Claims 1, 6, 11, 15, and 19 have been amended to incorporate a limitation that the parasitic information comprises both capacitance and resistance information. Support for this amendment may be found, for example, in Paragraph [0023] of the Specification. Accordingly, no new matter has been added by way of these amendments.

Claims 12-14 have been amended to correct a typographical error noticed by the Applicant. More specifically, claims 12-14 have been amended to recite "computer system"

instead of "method" because they depend from claim 11, which is directed towards a "computer system."

III. Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1, 4, 6, 9, 11, 13, 15-17, and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,610,833 (the '833 patent) issued to Chang et al. To the extent that the rejection still applies to the amended claims, the rejection is respectfully traversed.

Independent claims 1, 6, 11, 15, and 19 have been amended to incorporate the limitation that the parasitic information comprises *both* capacitance and resistance information. *See* Paragraph [0023] of the Specification. The '833 patent, on the other hand, discloses using a field solver to generate capacitance information *only*. *See* '833 patent, lines 60-67 and Figure 1a (block 112). In other words, the '833 patent discloses a tool using a capacitance simulator, not one that generates both capacitance and resistance information. This is significant because since the issuance of the '833 patent, process technologies of interconnects have changed (e.g., longer metal routings and increased numbers of metal layers) such that resistance information, in addition to capacitance information, is critical in accurate parasitic extraction. Accordingly, the '833 patent fails to show or suggest each and every element of amended claims 1, 6, 11, 15, and 19. Thus, Applicant respectfully requests withdrawal of the § 102 rejections. Claim 4 (which depends from claim 1), claim 9 (which depends from claim 6), claim 13 (which depends from claim 11), and claims 16 and 17 (which depend from claim 15) are patentable for at least the same reasons.

IV. Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 2, 7, and 12 under 35 U.S.C. § 103(a) as being unpatentable over the '833 patent. Because the '833 patent fails to show or suggest the limitations recited in claims 1, 6, and 11, claims 2, 7, and 12, which depend from these claims are likewise patentable. Thus, Applicant respectfully requests withdrawal of the § 103 rejection of claims 2, 7, and 12.

it does at column 5 lines 49-64

The Examiner rejected claims 3 and 8 under 35 U.S.C. § 103(a) as being unpatentable over the '833 patent in view of U.S. Patent No. 5,629,860 (the '860 patent) issued to Jones et al. The '860 patent does not show or suggest using a field solver to obtain both capacitance and resistance information as recited in the amended claims. Accordingly, the combination of the '833 patent and the '860 patent do not render claims 3 and 8 obvious. Therefore, Applicant respectfully requests withdrawal of the § 103 rejection of claims 3 and 8.

The Examiner rejected claims 5, 10, 14, and 18 under 35 U.S.C. § 103(a) as being unpatentable over the '833 patent in view of U.S. Patent No. 5,706,206 (the '206 patent) issued to Hammer et al. Because the '206 patent does not show or suggest using a field solver to obtain both capacitance and resistance information, and because amended independent claims 1, 6, 11, and 15 have been shown to be allowable over the '833 patent, Applicant respectfully requests withdrawal of the § 103 rejection of claims 5, 10, 14, and 18, which depend from the allowable independent claims.

V. New Claims

New claim 20 recites that the interconnect configuration of claim 1 can be non-symmetrical. As shown by Figure 1 and Equations (1)-(4) of the instant application, symmetry between different metal layers is not assumed. In other words, an interconnect configuration to the right of a particular metal routing is not assumed to be identical to the interconnect configuration to the left of that particular metal routing. Contrastingly, the '833 patent is directed toward and dependent on a symmetrical interconnect configuration, such as that shown in Figure 3 and by Equation 1 of the '833 patent. Accordingly, Applicant respectfully requests that the Examiner enter and allow new claim 20.

VI. Conclusion

The claims have been shown to be allowable over the prior art. Applicant believes that this paper is responsive to each and every ground of rejection cited by the Examiner in the Action dated May 8, 2002, and respectfully request favorable action in the form of a Notice of Allowance.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.102001/P5991).

Respectfully submitted,

Date: 8/8/02

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Jeffrey S. Bergman

Jonathan P. Osha, Reg. No. 33,986
Rosenthal & Osha L.L.P.
One Houston Center, Suite 2800
1221 McKinney Street
Houston, TX 77010

Telephone: (713) 228-8600
Facsimile: (713) 228-8778

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APPENDIX A – MARKED-UP VERSION OF THE AMENDED CLAIMS

1. (Amended) A method for creating a wire load model, comprising:

creating an interconnect configuration;

running a field solver to generate parasitic information for the interconnect configuration;

storing the parasitic information in an accessible format, wherein the parasitic information comprises capacitance and resistance information; and

running a curve-fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information.

6. (Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for creating a wire load model, the method comprising:

creating a wire structure;

running a field solver to generate parasitic information for the wire structure, wherein the parasitic information comprises capacitance and resistance information;

storing the parasitic information in an accessible format; and

running a curve-fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information.

11. (Amended) A computer system, comprising:

a memory for storing a model of a circuit;

a processor for creating a wire load model, wherein the processor establishes an interconnect configuration for the circuit;

a field solver for determining parasitic information for the interconnect configuration, wherein the parasitic information comprises capacitance and resistance information; and

a curve-fitting engine that uses the parasitic information to generate the wire load

model.

12. (Amended) The [method]computer system of claim 11, wherein a width and a spacing for the interconnect configuration is chosen so that the width and spacing is larger than a minimum width and spacing specification for the interconnect configuration.

13. (Amended) The [method]computer system of claim 11, wherein the curve-fitting engine is a non-linear curve-fitting engine.

14. (Amended) The [method]computer system of claim 11, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

15. (Amended) A method for creating a wire load model, comprising:

creating an interconnect configuration;

generating parasitic information for the interconnect configuration, wherein the parasitic information comprises capacitance and resistance information;

storing the parasitic information in an accessible format; and

creating the wire load model dependent on the parasitic information.

19. (Amended) A wire load model creation tool, comprising:

means for creating an interconnection configuration for a structure;

means for field solving the interconnect configuration to determine parasitic information, wherein the parasitic information comprises capacitance and resistance information;

means for storing the parasitic information;

curve-fitting means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model; and

means for controlling error in the curve-fitting means.